REMARKS

Applicant requests reconsideration of the above-identified application in light of the amendments and remarks described herein. Claims 1-41 were pending in this application, with Claims 27-41 being preliminarily withdrawn from consideration. Claims 1, 3, 5, 8, 11-18, 20-22, 25, and 26 have been amended, and Claims 27-41 have been cancelled. Therefore, Claims 1-26 are now pending in this application.

Claims 1-26 have been rejected. Specifically, Claims 1-26 have been rejected under 35 U.S.C. § 112, Claims 11-13 and 15-26 have been rejected under 35 U.S.C. § 102(b), and Claims 1-10 and 14 have been rejected under 35 U.S.C. § 103(a).

Applicant respectfully submits that all claims are now in condition for allowance. Accordingly, applicant requests reconsideration and allowance of all claims.

Summary

The present invention provides processes and tools for producing features that serve as precursors of solder bumps. Such precursors, when heated to a reflow temperature, form an alloyed solder bump.

Device manufacturers wishing to use flip chip technology as a packaging solution will find the processes and tools of the present invention useful in forming lead-free solder bumps that facilitate high density bonding and gang bonding along with suitable electrical performance, self-alignment, and reliability characteristics. By employing the processes and utilizing the tools of the present invention, device manufacturers can avoid the toxicity issues associated with lead-based solders while taking advantage of the ability of the present invention to control the composition of the solder alloy and deposit the constituents of the solder alloy at an acceptable deposition rate. Additionally, the baths from which the components of the solder alloy precursor are deposited are simple to maintain and are relatively stable. Each of the above features of the

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present invention will contribute to the device manufacturer's ability to cost effectively produce solder bumps.

In one embodiment, a precursor of a solder alloy is formed on a microelectronic workpiece by first forming a diffusion barrier layer (e.g., copper or nickel stud) on a surface of the microelectronic workpiece. The diffusion barrier layer inhibits diffusion of materials on one side of the diffusion barrier layer into materials that are on the other side of the diffusion barrier layer, and protects underlying seed layer from being consumed when the materials around the diffusion barrier layer are heated to a reflow temperature. Thereafter, a lead-free first conductive layer is formed over the diffusion barrier layer so that the diffusion barrier layer is located between the first conductive layer and the surface of the microelectronic pieces. A second lead-free conductive layer is then formed over the first conductive layer so that the first conductive layer is located between the second conductive layer and the diffusion barrier layer. The first and the second conductive layers are formed from different materials, for example, the first conductive layer can be silver and the second conductive layer can be tin.

Response to Restriction Requirement

The Office Action sets forth the position that the application contains two patentably distinct inventions defined by Group I (Claims 1-26) and Group II (Claims 27-41). Applicant confirms the election of Group I (Claims 1-26) for prosecution on the merits, which was made by Jeffrey Sakoi during a telephone conversation with the Examiner on February 26, 2007. Such election is made without traverse and without prejudice to file divisional applications on other noted inventions.

Objections to the Specification

The Office Action states that the title of the invention is not descriptive, and therefore, a new title is required that is clearly indicative of the invention to which the claims are directed.

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Applicant has amended the title to recite "PROCESSES FOR FORMING LEAD-FREE ALLOY SOLDER PRECURSORS ON MICROELECTRONIC WORKPIECES."

Claim Rejections Under 35 U.S.C. § 112, First Paragraph

Claims 1-26 stand rejected under 35 U.S.C. § 112, first paragraph. Specifically, the Office Action states that the specification, while being enabling for electrolytic coating and plating, does not reasonably provide enablement for other forms of coating and plating, such as immersion, electroless, spraying, laminated, etc. Applicant respectfully submits that the specification does enable other forms of coating and plating, such as substitutional reduction (see page 8, line 31, to page 9, line 6), sputtering (see page 5, lines 4-6), and conventional electrochemical deposition techniques, such as electrolytic or electroless processes (see page 5, lines 15-17). Therefore, applicant respectfully requests withdrawal of the rejection.

Claims 1-26 further stand rejected under 35 U.S.C. § 112, first paragraph. Specifically, the Office Action states that the formation of a patterned mask atop the barrier layer prior to forming the multiple conductive layers as well as the reflowing of two conductive layers to form the solder bump are critical or essential to the practice of the invention, but are not included in the claims. Regarding reflowing the conductive layers to form the solder bump, applicant submits that the claims are directed to a process of forming a solder alloy precursor, i.e., before reflow.

Regarding the formation of a patterned mask atop the barrier layer prior to forming the multiple conductive layers, applicant directs the Examiner to the preamble of Claim 1:

> A process of forming a solder alloy precursor on a microelectronic workpiece that includes a patterned mask over a conductive under bump metallurgy, the patterned mask exposing portions of the conductive under bump metallurgy . . . .

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Regarding the remaining independent claims, Claims 11, 16, and 21, as amended, recite the following language:

> A process of forming a solder alloy precursor on a microelectronic workpiece comprising:
>
> forming one of a patterned mask and a diffusion barrier layer over a conductive under bump metallurgy;
>
> forming the other of the patterned mask and the diffusion barrier layer, wherein the pattered mask is formed on the diffusion barrier layer and wherein the diffusion barrier layer is formed on the exposed portions of the conductive under bump metallurgy . . . .

Accordingly, applicant respectfully requests withdrawal of the rejections to these claims.

Claim Rejections Under 35 U.S.C. § 112, Second Paragraph

Claims 3, 5, 8, 12, 13, 15, 17, 18, 20, 22, 25, and 26 stand rejected under 35 U.S.C. § 112, second paragraph. Specifically, the Examiner states that these claims recite improper Markush terminology. Applicant has made appropriate amendments to the claims.

Claim Rejections Under 35 U.S.C. § 102(b): Hur Fails to Teach, or Even Suggest, Each and Every Claim Element of Claims 11-13 and 15-26

Claims 11-13 and 15-26 stand rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 6,013,572, issued to Hur et al. (hereinafter "Hur"). Applicant disagrees.

Anticipation requires the presence of each and every claim element in a single prior art reference. Hur fails to teach, or even suggest, each and every element of the claims at issue.

Hur is generally directed to a method of fabricating tin-silver solder bumps. Hur describes plating silver on the exposed portions of the under bump metallurgy, plating tin onto the silver, and reflowing to form tin-silver alloy solder bumps. The Office Action admits on page 6 that Hur fails to teach forming a diffusion barrier layer on the UBM layer underneath the solder material.

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Claims 11, 16, and 21, as currently amended, recite "A process of forming a solder alloy precursor on a microelectronic workpiece comprising: forming one of a patterned mask and a diffusion barrier layer over a conductive under bump metallurgy; forming the other of the patterned mask and the diffusion barrier layer, wherein the pattered mask is formed on the diffusion barrier layer and wherein the diffusion barrier layer is formed on the exposed portions of the conductive under bump metallurgy . . . ."

In view of the Office Action admission that Hur fails to teach forming a diffusion barrier layer on the UBM layer underneath the solder material, applicant submits that Hur fails to teach or suggest each and every element of Claims 11, 16, and 21, and Claims 12-15, 17-20, and 22-26 depending therefrom. Accordingly, applicant respectfully requests withdrawal of the rejections to these claims.

Claim Rejections Under 35 U.S.C. § 103(a):

Hur and Mitchell Fail to Teach or Suggest All of the Claim Limitations of Claims 1-10 and 14

Claims 1-10 and 14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hur in view of U.S. Patent No. 5,773,359, issued to Mitchell et al. (hereinafter "Mitchell"). Applicant disagrees.

To establish a case of obviousness, the prior art references must teach or suggest all of the claim limitations; there must be some suggestion or motivation, either in the references or in the knowledge of one skilled in the art, to modify the references or to combine the reference teachings; and there must be a reasonable expectation of success. Hur and Mitchell, either alone or in any combination, fail to teach or suggest all of the claim limitations of the claims at issue.

Mitchell is generally directed to an interconnect system, including an interconnect bump over an under bump metallurgy and the method of fabricating the same. Mitchell describes under bump metallurgy including three layers: a barrier layer 26 (e.g., titanium, tungsten, nickel,

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or chrome); an adhesion layer 28 (e.g., copper); and a mixture layer 27, which is a mixture of the material of the barrier layer 26 and the material of the adhesion layer 28 (e.g., titanium copper) to serve as a transition layer between layers 26 and 28.

Claim 1, as currently amended, recites "A process of forming a solder alloy precursor on a microelectronic workpiece . . . wherein the first conductive layer does not include material from one of the second conductive layer and the diffusion barrier layer."

The cited references fail to teach or suggest all of the elements of Claim 1. As mentioned above, Hur fails to teach forming a diffusion barrier layer on the UBM layer underneath the solder material. Mitchell teaches a barrier layer 26, as well as an adhesion layer 28 and a mixture layer 27. However, Mitchell teaches that the mixture layer 27 is located between layers 26 and 28 and contains a mixture of the barrier material of layer 26 and the adhesion material of layer 28. Therefore, the references, whether cited alone or in combination, fail to teach that the first conductive layer does not include material from one of the second conductive layer and the diffusion barrier layer, as recited in Claim 1 and Claims 2-10 depending therefrom. Accordingly, applicant respectfully requests withdrawal of the rejections to these claims.

Regarding the rejection of Claim 14, applicant respectfully submits that the cited references, whether cited alone or in combination, fail to teach or suggest at least one additional conductive layer (i.e., at least a third conductive layer), wherein the at least one additional conductive layer has a different composition than the second conductive layer, as recited in amended Claim 14. Accordingly, applicant also requests withdrawal of the rejection to Claim 14.

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Conclusion

In view of the foregoing amendments and remarks, applicant respectfully submits that the present application is in condition for allowance. The Examiner is invited to contact the undersigned with any remaining questions or concerns.

Respectfully submitted,

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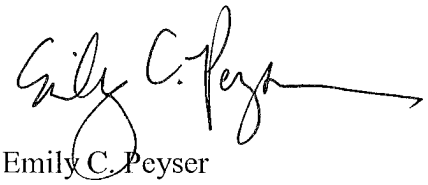

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